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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No.0325.00379
Date: June 28, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Kevin Gallagher, Gerald Donal Murphy and Anthony Gerard Dunne

For: REFERENCE-SWITCH HYSTERESIS FOR COMPARATOR APPLICATIONS

Enclosed are:

1. X Specification (15 pages); Claims (6 pages); Abstract (1 page)

2. X 4 sheets of formal drawings.

3. X Oath or Declaration Total Pages 3
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$690.00
Total Claims	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $690.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $730.00

X A check in the amount of $730.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

Correspondence Address:

Customer Number or Bar Code Label: 21363

PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL573624558US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on June 28, 2000.

By: Mary Donna Berkley

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Respectfully submitted,

By _____

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REFERENCE-SWITCH HYSTERESIS FOR COMPARATOR APPLICATIONS

Field of the Invention

The present invention relates to a method and/or architecture for hysteresis in a comparator generally and, more particularly, to a method and/or architecture for a reference-switch hysteresis for comparator applications.

Background of the Invention

Conventional approaches for comparator designs implement hysteresis utilizing a form of positive feedback. Traditionally, hysteresis that is incorporated into a design using positive feedback does not provide accurately or efficiently controlled hysteresis. Hysteresis is the measure for a comparator for which an input threshold changes as a function of the input (or output) level. More specifically, when the input passes the input threshold, the output changes state and the input threshold is subsequently reduced so that the input must return beyond the initial input threshold before the output of the comparator changes state again.

Such conventional implementations are dependent on temperature and process variations resulting in an uncontrolled amount of hysteresis. An example of one conventional approach can be found in U.S. Patent 4,072,870 entitled "Comparison circuit having programmable hysteresis", which is hereby incorporated by reference in its entirety. The conventional approach of U.S. Patent 4,072,870 implements a steering current through a resistor to produce symmetrical hysteresis. However, the conventional approach does not present accurate or efficiently controlled hysteresis.

Summary of the Invention

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to generate a reference output voltage in response to a plurality of reference voltages. The second circuit may be configured to generate an output voltage in response to the reference output voltage and an unknown voltage. The output voltage may comprise accurately controlled hysteresis.

The objects, features and advantages of the present invention include providing a method and/or architecture for

implementing reference-switch hysteresis in comparator applications that may (i) implement different voltage reference levels to produce an effective amount of hysteresis, (ii) provide an accurate and constant amount of hysteresis, (iii) provide bandgap controlled reference voltages levels, (iv) provide immunity against temperature, supply and process corner variations and/or (v) provide controlled and accurate reference voltage levels, resulting in a controlled and accurate amount of hysteresis.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram of the present invention;

FIG. 3 is a detailed block diagram of an alternate embodiment of the present invention;

FIG. 4 is a detailed block diagram of an alternate embodiment of the present invention;

FIG. 5 is a detailed block diagram of an alternate embodiment of the present invention;

FIG. 6 is a detailed block diagram of an alternate embodiment of the present invention; and

FIG. 7 is a detailed block diagram of an alternate embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented to provide reference switched hysteresis (e.g., on chip bias voltage switched hysteresis), for example, in comparator applications. The circuit 100 may provide immunity against temperature, supply and process corner variations. Additionally, the circuit 100 may provide controlled and accurate reference voltage levels (e.g., on chip bias voltages), resulting in a controlled and accurate amount of hysteresis. The structure of the circuit 100 generally comprises a voltage generator block (or circuit) 102 and a comparator block (or circuit) 104.

The voltage generator circuit 102 may have an output 106 that may present a signal (e.g., VREF) and an input 110 that may receive the signal (e.g., OUT). The signal VREF may be implemented as a reference voltage, a voltage level, a voltage on a node or other appropriate signal in order to meet the criteria of a particular implementation. The comparator circuit 104 may have an input 108 that may receive the signal VREF, an input 112 that may receive a signal (e.g., VX) and an output 114 that may present the signal OUT. In one example, the signal VREF may provide a bandgap controlled reference voltage to the comparator 104. The bandgap controlled reference voltage may be implemented to control hysteresis of the comparator 104. The signal VX may be implemented as a voltage level, a voltage on a node or other appropriate signal in order to meet the criteria of a particular implementation. However, a particular voltage level of the signal VX may be unknown. For example, the signal VX may be received from another circuit (e.g., VX may be the input to a low-battery detect circuit).

The circuit 100 may provide accurate hysteresis control external to the comparator 104 (e.g., the voltage generator circuit 102). The circuit 100 may allow the comparator 104 to have a

minimal amount of hysteresis to provide a robust design. However, the amount of hysteresis of the comparator 104 may be required to be smaller than an overall hysteresis of the circuit 100, in order to ensure accurately controlled hysteresis. The voltage generator 102 may present the signal VREF by switching between a number of internal voltages. The voltage generator 102 may generate the signal VREF to provide the required hysteresis (to be described in more detail in connection with FIG. 2). The circuit 100 may provide accurate control over a variety of hysteresis levels (via the signal OUT). Alternatively, the signal OUT may be presented to a digital filter (not shown) for further processing. The digital filter may be optionally implemented to meet the design criteria of a particular implementation.

Referring to FIG. 2, a more detailed diagram of the circuit 100 is shown. The voltage generator 102 generally comprises a circuit (or block) 120, a circuit (or block) 122 and a circuit (or block) 124. The circuit 120 may be implemented as a bandgap reference circuit. The circuit 122 may be implemented as a voltage reference generator circuit. The circuit 124 may be implemented as a reference switch circuit. The circuit 120 generally presents a signal (e.g., SUM) to the circuit 122. The

circuit 120 generally comprises a positive temperature coefficient circuit (or block) 128, a summing circuit (or block) 130 and a negative temperature coefficient circuit (or block) 132.

The positive temperature coefficient circuit 128 may generate a signal (e.g., KVT). The signal KVT may be presented to the summing circuit 130. The negative temperature coefficient circuit 132 may present a signal (e.g., VBE) to the summing circuit 130. In one example, the signal VBE may be implemented as a negative temperature coefficient voltage. Additionally, the signal VBE may be generated by a diode connected bipolar device. The negative temperature coefficient circuit 132 generally comprises a current source 134 and a diode 136. However, other appropriate circuits may be implemented accordingly to meet the design criteria of a particular implementation. The current source 134 may be coupled to a first side of the diode 136. A second side of the diode 136 may be coupled to ground. Additionally, the current source 134 and the diode 136 may be configured to generate the signal VBE.

The summing circuit 130 generally sums the signal VBE and the signal KVT. The summing circuit 130 may generate the signal SUM. The signal SUM may be implemented as a summation signal. In

one example, the signal SUM may be implemented as a control voltage. In another example, the signal SUM may be implemented as a control current. However, the signal SUM may be implemented as another appropriate signal in order to meet the criteria of a particular implementation.

The circuit 122 generally comprises a current source (or generator) I1, a current source (or generator) I2, a resistor R1 and a resistor R2. The circuit 100 (of FIG. 2) illustrates two reference current sources (e.g., I1 and I2). However, another number of current sources may be implemented in order to meet the design criteria of a particular application.

In one example, the current sources I1 and I2 may be implemented as voltage controlled current sources (VCCS). In another example, the current sources I1 and I2 may be implemented as current controlled sources (CCCS). However, the current sources I1 and I2 may be implemented as other appropriate current sources in order to meet the criteria of a particular implementation.

Each of the current sources I1 and I2 may be coupled to a first side of the resistors R1 and R2, respectively. A second side of the resistors R1 and R2 may be coupled to ground. The current sources I1 and I2 generally receive the signal SUM. The

signal SUM may control the current sources I1 and I2. The current source I1 generally presents a signal (e.g., VREF1) and the current source I2 generally presents a signal (e.g., VREF2). The signals VREF1 and VREF2 may be implemented as a reference voltage, a voltage level, a voltage on a node, or other appropriate signals in order to meet the criteria of a particular implementation. The current source I1 and the resistor R1 may control the voltage level of the signal VREF1 in response to the signal SUM. The current source I2 and the resistor R2 may control the voltage level of the signal VREF2 in response to the signal SUM. The signals VREF1 and VREF2 are generally presented to the reference switch circuit 124.

The reference switch circuit 124 generally presents the signal VREF to the comparator circuit 104. Additionally, the reference switch circuit 124 may receive the signal OUT. In one example, the signal OUT may be implemented as a feedback signal. The signal OUT may control switching of the reference switch 124. Additionally, the signal OUT may control the voltage level of the signal VREF. The reference switch circuit 124 generally comprises a switch S1 and a switch S2. The signal VREF1 may be presented to a first side of the switch S1. A second side of the switch S1 may be connected to the output 106 (e.g., the node VREF). The signal

VREF2 may be presented to a first side of the switch S2. A second side of the switch S2 may be connected to the output 106 (e.g., the node VREF). The switch S1 and the switch S2 may be controlled by the signal OUT. The switches S1 and S2 may control the voltage level of the signal VREF.

The bandgap reference circuit 120 generally controls the current sources I1 and I2 via the signal SUM. The current generator I1 and the resistor R1 may control the reference voltage level VREF1, where VREF1 is generally equal to I1*R1. The current source I2 and the resistor R2 may control the reference voltage level VREF2, where VREF2 is generally equal to I2*R2. The resistors R1 and R2 may have the same characteristics (e.g., resistance) as resistors (not shown) within the bandgap reference circuit 120. The bandgap reference circuit 120 may control the voltage reference levels VREF1 and VREF2. The voltage reference levels VREF1 and VREF2 may be accurately controlled (e.g., process corners, supply and temperature independent) via the bandgap reference circuit 120.

The signal VREF is generally switched to be equal to either the signal VREF1 or the signal VREF2. The signal VREF may be switched in response to the feedback signal OUT. The reference

switch circuit 124 may be implemented to provide an appropriate voltage level of the signal VREF. Switching of the signal VREF may provide a controlled amount of hysteresis. The signal VREF is generally presented to the input 108 of the comparator block 104. Additionally, the signal VX is generally presented to the input 112 of the comparator block 104. The comparator block 104 generally comprises a comparator 132. A positive input of the comparator 132 may receive the signal VREF and a negative input of comparator 132 may receive the signal VX. The comparator 132 may compare the signal VREF and the signal VX. Additionally, the comparator 132 may generate the signal OUT. The comparator 132 may generate the signal OUT in response to a voltage level of the signal VREF and a voltage level of the signal VX.

Additionally, the circuit 100 may optionally comprise a circuit 140. The circuit 140 may be implemented as a capacitance block (or circuit). The circuit 140 may be optionally implemented to control a voltage level of the signal VREF. The circuit 140 generally comprises a capacitor C1. A first side of the capacitor C1 may be coupled to the node VREF. A second side of the capacitor C1 may be coupled to ground. A capacitance of the capacitor C1 may

be varied in order to meet the criteria of a particular implementation.

Referring to FIG. 3, an alternate embodiment of the present invention is shown marked with primed notation. The circuit 100' may be similar to the circuit 100. The circuit 100' illustrates a scheme to generate two or more references from a bandgap voltage reference.

Referring to FIG. 4, an alternate embodiment of the present invention is shown marked with double primed notation. The circuit 100'' may be similar to the circuit 100. The circuit 100'' may illustrate an implementation where the voltages VREF1 and VREF2 are directly generated by the bandgap circuit 110''. The circuit 100'' illustrates an example that uses a bandgap in which the bandgap voltage is already across a resistor divider and so multiple VREFs are available. No additional operational amplifier is required.

Referring to FIG. 5, an alternate embodiment of the present invention is shown marked with triple primed notation. The circuit 100''' may be similar to the circuit 100. The circuit 100''' may be useful to distribute VREFs via currents to avoid grounding problems.

Referring to FIG. 6, an alternate embodiment of the present invention is shown marked with quadruple primed notation. The circuit 100'''' may be similar to the circuit 100. The circuit 100'''' may implement the bandgap voltage that does not have a high gain. The circuit 100'''' may be usable for low levels of VREF1 and VREF2.

Referring to FIG. 7, an alternate embodiment of the present invention is shown marked with five primed notations. The circuit 100''''' may be similar to the circuit 100. The circuit 100''''' may implement positive (+ve) TC and negative (-ve) TC currents that are summed. The choice of the resistance R makes VREF ~ (K2/R2)*(VGO).

The circuit 100 may provide accurately controlled hysteresis, external to a comparator (e.g., via the voltage generator 102). The circuit 100 may implement a number of reference voltages (e.g., VREF1 and VREF2) to provide the accurately controlled hysteresis. When switched appropriately by the switches S1 and S2, the circuit 100 may provide a controlled amount of hysteresis via switching of the signal VREF.

The bandgap reference circuit 120 may be implemented to provide temperature, supply and process independent signals (e.g.,

VREF1 and VREF2). However, the voltage reference levels VREF1 and VREF2 may only be as accurate as the bandgap reference circuit 120. The bandgap reference circuit 120 may allow the circuit 100 to provide voltage levels that may be stable over temperature, supply process corners. However, other sources of reference may also be implemented to meet the design criteria of a particular implementation. For example, a Zener reference may be implemented with a buffer and a resistor divider.

The circuit 100 may implement bandgap-controlled voltage reference levels (e.g., VREF1 and VREF2) to produce an effective amount of hysteresis (on the signal OUT). The hysteresis on the signal OUT may be equal to the difference between the reference levels VREF1 and VREF2. The circuit 100 may be implemented where an accurate and dependable amount of hysteresis is required. The circuit 100 may provide voltage reference levels that may be bandgap controlled, offering immunity against temperature, supply and process corner variations. The bandgap generated voltage reference levels may be used to provide stable references over temperature, supply and process corners. Since the reference levels may be accurately controlled, the circuit 100 may provide a controlled and accurate amount of hysteresis. The circuit 100 may

be implemented where the control of hysteresis levels is of primary importance.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a first circuit configured to generate a reference output voltage in response to a plurality of reference voltages; and

a second circuit configured to generate an output voltage in response to said reference output voltage and an unknown voltage, wherein said output voltage comprises accurately controlled hysteresis.

2. The apparatus according to claim 1, wherein said first circuit comprises a voltage generator circuit and said second circuit comprises a comparator.

3. The apparatus according to claim 1, wherein first circuit is configured to switch between said plurality of reference voltages.

4. The apparatus according to claim 3, wherein said first circuit is further configured in response to a feedback signal.

5. The apparatus according to claim 4, wherein said feedback signal comprises said output voltage.

6. The apparatus according to claim 1, wherein said first circuit is further configured in response to voltage, process and temperature variations.

7. The apparatus according to claim 1, wherein said first circuit comprises:

a bandgap reference circuit;

a voltage reference circuit configured to generate said plurality of reference voltages; and

a reference switch circuit configured to switch between said plurality of reference voltages to generate said output voltage.

8. The apparatus according to claim 7, wherein said bandgap reference circuit comprises:

a process/compensation circuit;

a reference circuit; and

a summation circuit configured to control said voltage reference circuit in response to signals from said process compensation circuit and said reference circuit.

9. The apparatus according to claim 7, wherein said voltage reference circuit comprises:

a plurality of current sources configured to generate said plurality of reference voltages; and

a plurality of resistors each coupled to at least one of said plurality of current sources.

10. The apparatus according to claim 7, wherein said reference switch circuit comprises:

a plurality of switches each (i) configured to receive at least one of said plurality of reference voltages and (ii) coupled to said reference output voltage.

11. The apparatus according to claim 10, wherein said plurality of switches are configured in response to said output voltage.

12. The apparatus according to claim 1, wherein said plurality of reference voltages comprise bandgap controlled voltages.

13. An apparatus comprising:

means for generating a reference output voltage in response to a plurality of reference voltages; and

means for generating an output voltage in response to said reference output voltage and an unknown voltage, wherein said output voltage comprises accurately controlled hysteresis.

14. A method for providing accurate and controlled hysteresis comprising the steps of:

(A) selecting a reference output voltage from a plurality of reference voltages; and

(B) generating an output voltage in response to said reference output voltage and an unknown voltage, wherein said output voltage comprises accurately controlled hysteresis.

15. The method according to claim 14, wherein step (A) further comprises:

switching between said plurality of reference voltages.

16. The method according to claim 14, wherein step (A) further comprises:

controlling a voltage level of said plurality of reference voltages.

17. The method according to claim 14, wherein step (A) is further responsive to a feedback signal.

18. The method according to claim 17, wherein said feedback signal comprises said output voltage.

19. The method according to claim 14, wherein step (B) is further responsive to voltage and temperature variations.

20. The method according to claim 14, wherein step (A) further comprises the sub-steps of:

(A-1) summing a positive temperature coefficient and a negative temperature coefficient; and

(A-2) controlling a voltage level of said plurality of reference voltages.

ABSTRACT OF THE DISCLOSURE

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to generate a reference output voltage in response to a plurality of reference voltages. The second circuit may be configured to generate an output voltage in response to the reference output voltage and an unknown voltage. The output voltage may comprise accurately controlled hysteresis.

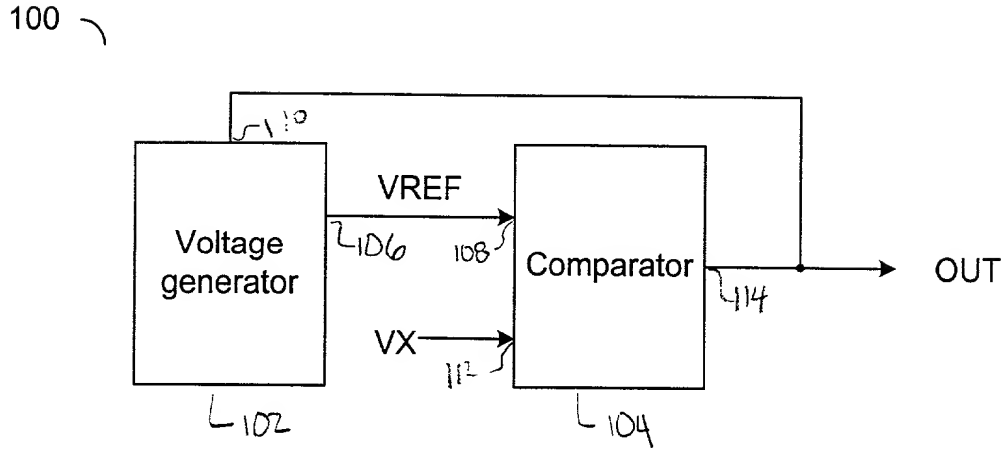
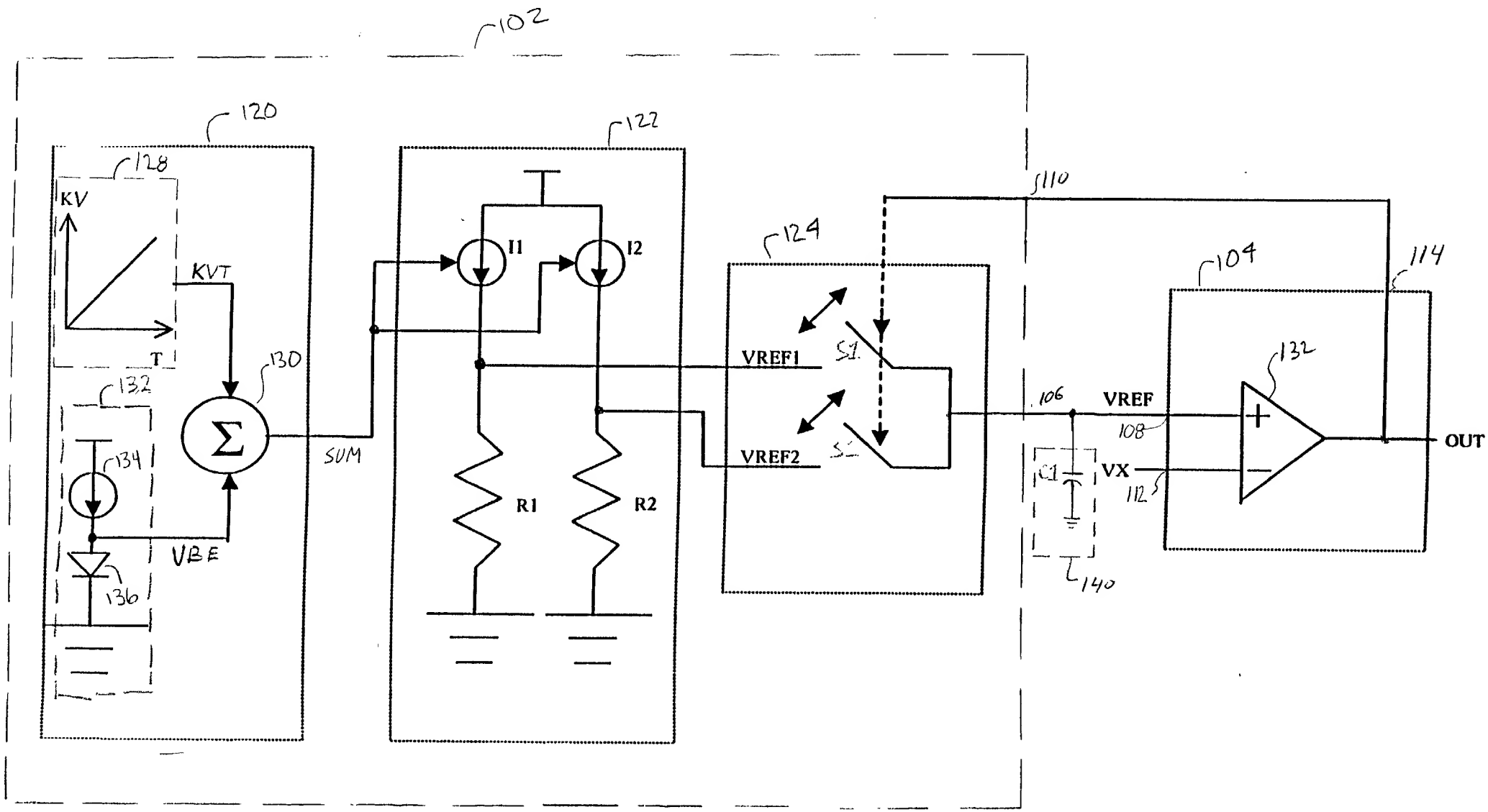

100
110
Voltage generator
VREF
106
108
Comparator
OUT
414
VX
112
102
104

FIG. 1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102
120
128
KV
KVT
T
130
132
134
136
VBE
SUM
122
I1
I2
R1
R2
124
VREF1
VREF2
S1
S2
110
106
VREF
108
VX
112
C1
140
104
132
114
OUT

FIG.2

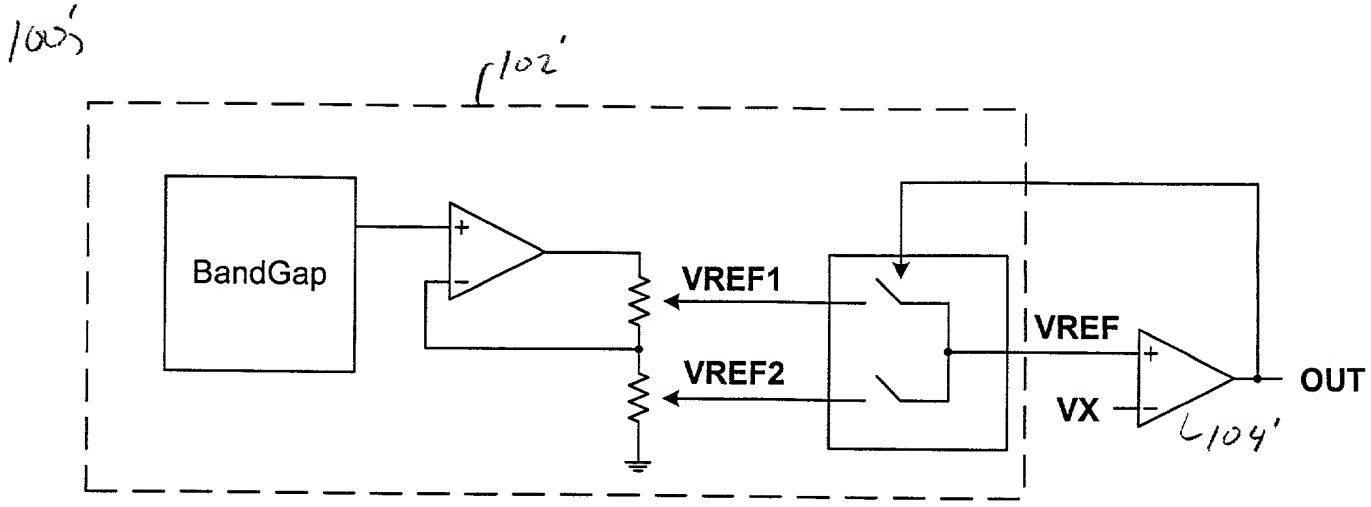

FIG.3

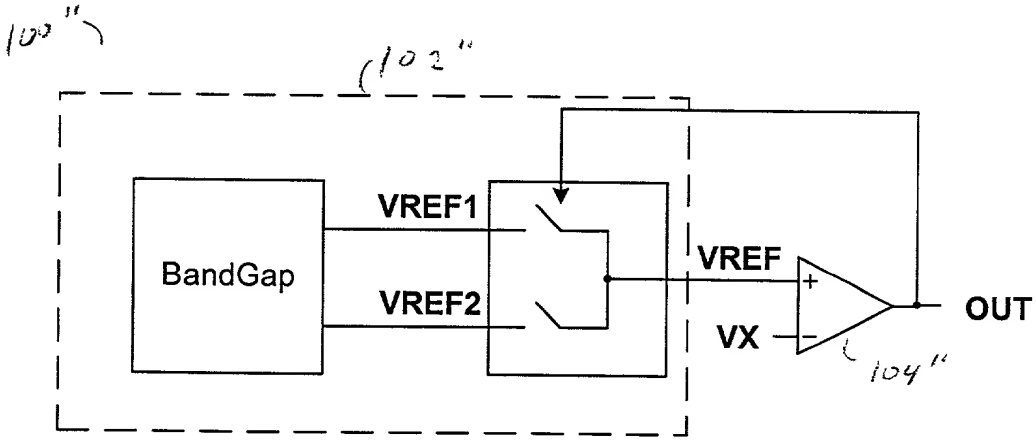

FIG.4

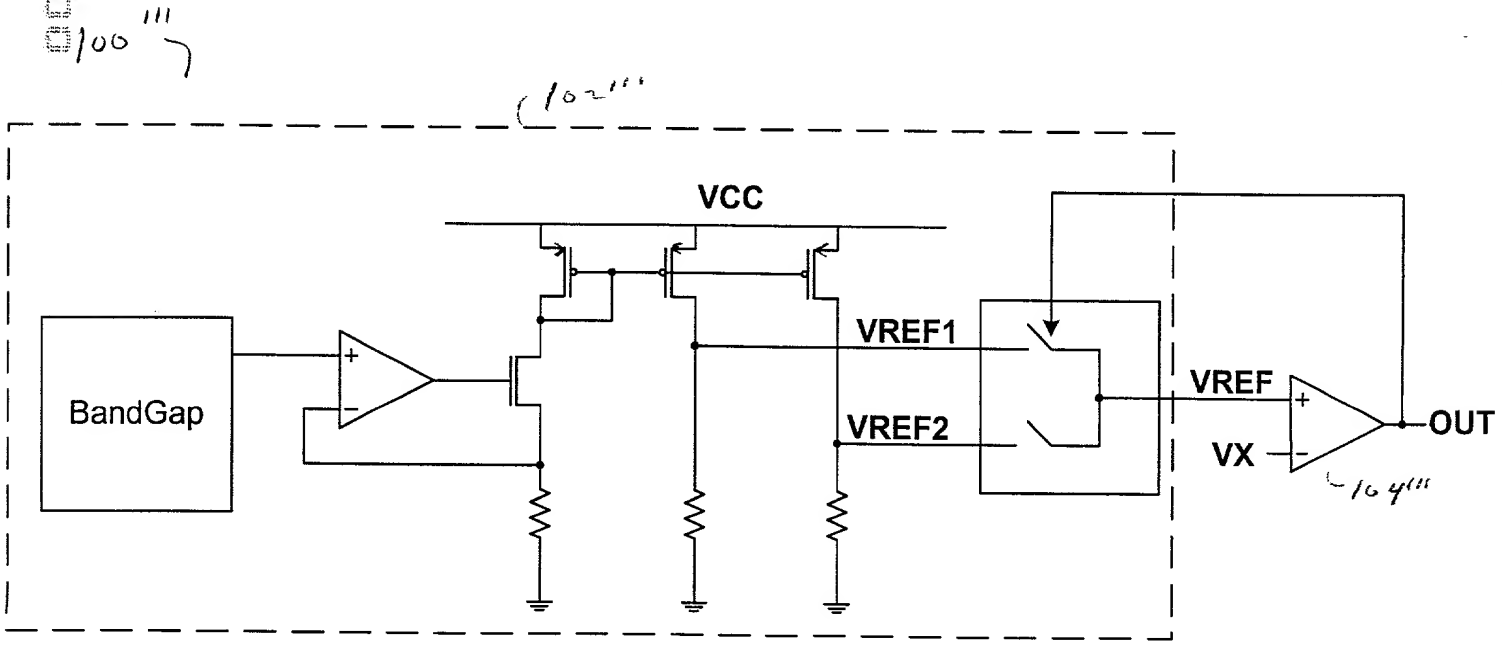

FIG.5

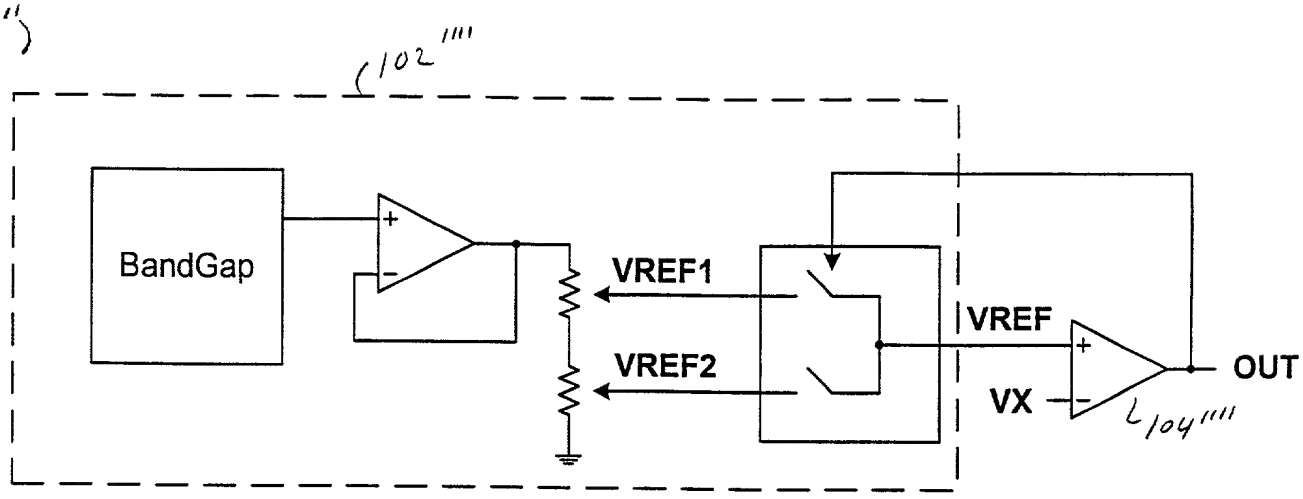
BandGap
VREF1
VREF2
VREF
VX
OUT

FIG.6

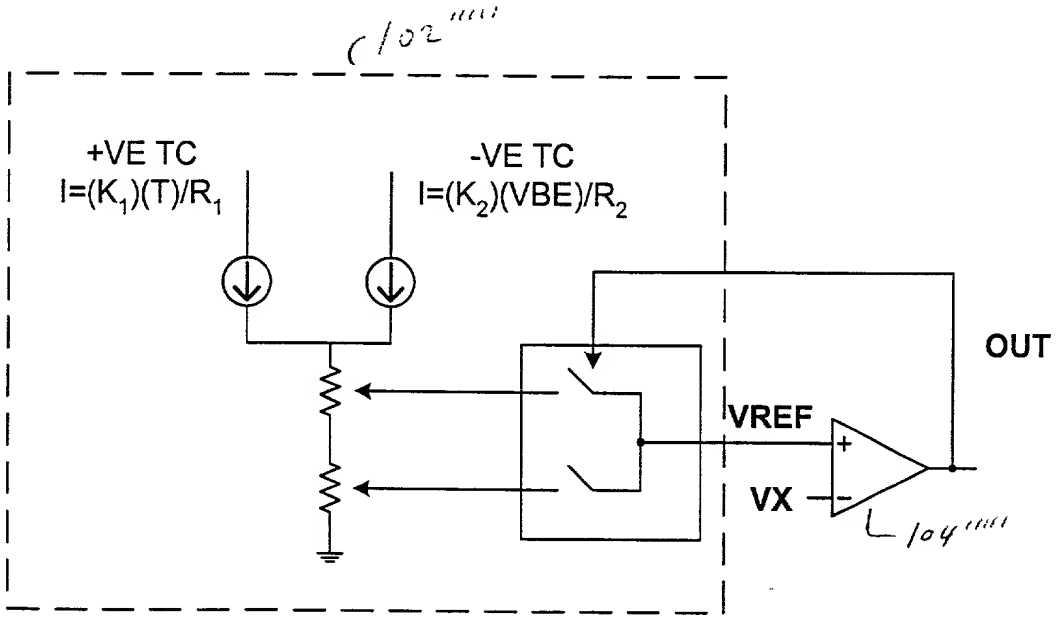
+VE TC
I=(K1)(T)/R1
-VE TC
I=(K2)(VBE)/R2
OUT
VREF
VX

FIG.7

Docket No. 0325.00379

DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled **"REFERENCE-SWITCH HYSTERESIS FOR COMPARATOR APPLICATIONS"**, which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

21363

PATENT TRADEMARK OFFICE

We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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Kevin Gallagher
Signature of First Joint Inventor

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Anthony Dunne
Signature of Third Joint Inventor

26 June
Date

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Citizen of: Ireland

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